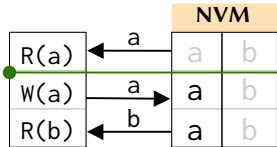
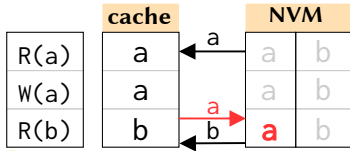


← NVM read access    ● checkpoint    x unmodified NVM  
 → NVM write access    → WAR violation    x modified NVM



1 Traditional intermittent system without data cache



2 Intermittent system with unsupported data cache