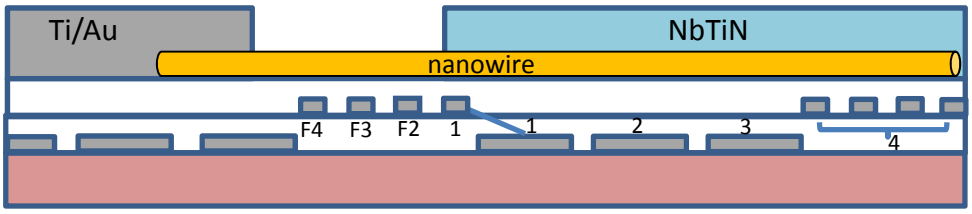
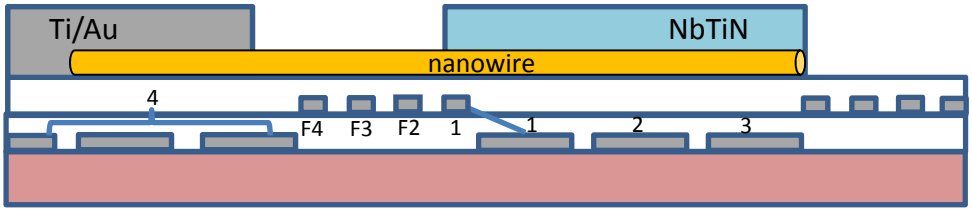
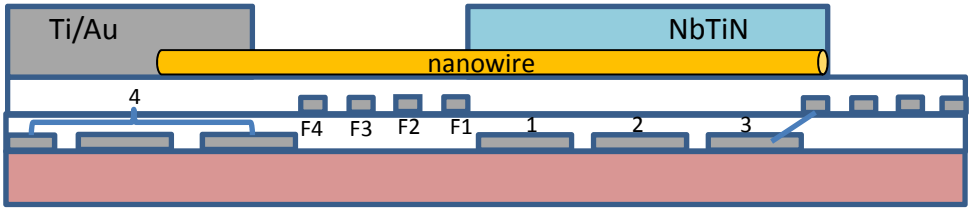
Gate layout N-nanowire-S device 1



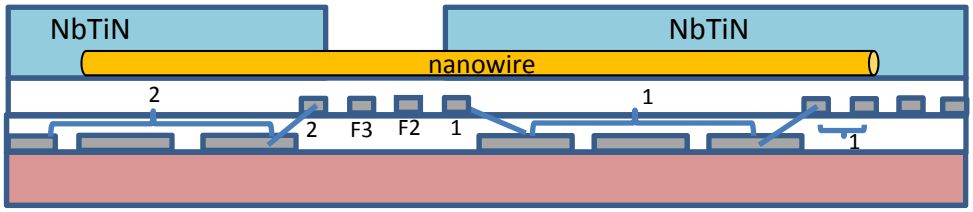

Gate layout N-nanowire-S device 2




Gate layout N-nanowire-S device 3




Gate layout S-nanowire-S device




Gate layout N-nanowire-N device